UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/634,851	08/06/2003	Jun Kanamori	MAE 292	7005

23995 7590 02/28/2006

RABIN & Berdo, PC
1101 14TH STREET, NW
SUITE 500
WASHINGTON, DC 20005

EXAMINER	
ISAAC, STANETTA D	

ART UNIT	PAPER NUMBER
2812	

DATE MAILED: 02/28/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

EK

Office Action Summary	Application No.	Applicant(s)	
	10/634,851	KANAMORI, JUN	
	Examiner	Art Unit	
	Stanetta D. Isaac	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 December 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6,8-13 and 17-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,8-13 and 17-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

LYNNE A. GURLEY
PRIMARY PATENT EXAMINER
TC 2800, AU 2812

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the amendment filed on 12/06/05. Currently, claims 1-6, 8-13 and 17-23 are pending.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 4-6, 8, 11-13 and 17-23 are rejected under 35 U.S.C. 102(e) as being anticipated by Yang et al., US Patent 6,686,255.

Yang discloses the semiconductor method as claimed. See figures 1-5, and corresponding text, where Yang teaches, pertaining to claim 1, a method of fabricating a semiconductor device, having a silicon layer disposed on an insulating film, the method comprising: oxidizing a surface of the silicon layer **14** to form a pad oxide film **16** (figure 1; col. 6, lines 6-11); passing oxygen ions **22** into an upper surface of the pad oxide film, and out of a lower surface of the pad oxide film to implant the oxygen ions into selected parts of the silicon layer that are in direct contact with the lower surface of the pad oxide film, directly under, and completely covered by the pad oxide film (figure 2; col. 7, lines 10-26); and oxidizing **24** the selected parts of the silicon layer, into which the oxygen ions have been implanted, and while the selected parts are still covered by the pad oxide film, to form isolation regions dividing the

silicon layer into a plurality of mutually isolated active regions (figures 3 and 4; col. 7, lines 38-64; col. 8, lines 52-65).

Yang teaches, pertaining to claim 4, wherein the isolation regions are field oxide regions (figure 4; col. 9, lines 12-28).

Yang teaches, pertaining to claim 5, wherein the implanted oxygen ions have a concentration that varies from an upper surface of the silicon layer to a lower surface of the silicon layer (col. 7, lines 18-26, ***Note***: the Examiner takes the position that the implanted oxygen ions would have a concentration that varies from an upper and lower surface of the silicon substrate and a concentration in a lower half of the silicon substrate, since the nature of the implantation will concentrate the ions in one part (upper or lower half) of the substrate vs. the other depending on the energy of the implant. Additionally, since silicon conventionally includes an oxygen concentration at room temperature of $2.5 \times 10^{15}/cm^3$, any additional oxygen ion implantation, within a specific region may combine with the implanted oxygen to further vary the concentration of the upper and lower surfaces of the substrate. See *Stanley Wolf and Richard N. Tauber, Silicon Processing For The VLSI Era, Vol. I, Second Edition, page 19, under 1.3.51 Oxygen and Carbon Measurements in Silicon Using Infrared Absorbance Spectroscopy*).

Yang teaches, pertaining to claim 6, wherein the implanted oxygen ions have a peak concentration in a lower half of the silicon layer (col. 7, lines 18-26, ***Note***: the Examiner takes the position that the implanted oxygen ions would have a concentration that varies from an upper and lower surface of the silicon substrate and a concentration in a lower half of the silicon substrate, since the nature of the implantation will concentrate the ions in one part (upper or lower half) of the substrate vs. the other depending on the energy of the implant. Additionally,

since silicon conventionally includes an oxygen concentration at room temperature of 2.5 x $10^{15}/cm^3$, any additional oxygen ion implantation, within a specific region may combine with the implanted oxygen to further vary the concentration of the upper and lower surfaces of the substrate. See *Stanley Wolf and Richard N. Tauber, Silicon Processing For The VLSI Era, Vol. I, Second Edition, page 19, under 1.3.51 Oxygen and Carbon Measurements in Silicon Using Infrared Absorbance Spectroscopy*).

Yang teaches, pertaining to claim 8, a method of fabricating a semiconductor device, having a silicon layer disposed on an insulating film, the method comprising: oxidizing a surface of the silicon layer **14** to form a pad oxide film **16** (figure 1; col. 6, lines 6-11); forming a first oxidation-resistant film **18a/b** on the pad oxide film **16** (figure 1; col. 5, lines 62-65; col. 6, lines 12-43); selectively removing the first oxidation-resistant film from parts of the silicon layer (figure 1; col. 6, lines 39-43); passing oxygen ions **22** into an upper surface of the pad oxide film, and out of a lower surface of the pad oxide film to implant the oxygen ions into the silicon layer, using remaining parts of the first oxidation-resistance film as a mask, the parts of the silicon layer having the oxygen ions implanted therein being in direct contact with the lower surface of the pad oxide film, directly under, and completely covered by the pad oxide film (figure 2; col. 7, lines 10-26); and oxidizing **24** the parts of the silicon layer into which the oxygen ions have been implanted, and while the parts are still covered by the pad oxide film, to form isolation regions dividing the silicon layer into a plurality of mutually isolated active regions (figures 3 and 4; col. 7, lines 38-64; col. 8, lines 52-65).

Yang teaches, pertaining to claim 11, wherein the isolation regions are field oxide regions (figure 4; col. 9, lines 12-28).

Yang teaches, pertaining to claim 12, wherein the implanted oxygen ions have a concentration that varies from an upper surface of the silicon layer to a lower surface of the silicon layer (col. 7, lines 18-26, ***Note***: the Examiner takes the position that the implanted oxygen ions would have a concentration that varies from an upper and lower surface of the silicon substrate and a concentration in a lower half of the silicon substrate, since the nature of the implantation will concentrate the ions in one part (upper or lower half) of the substrate vs. the other depending on the energy of the implant. Additionally, since silicon conventionally includes an oxygen concentration at room temperature of $2.5 \times 10^{15}/cm^3$, any additional oxygen ion implantation, within a specific region may combine with the implanted oxygen to further vary the concentration of the upper and lower surfaces of the substrate. See *Stanley Wolf and Richard N. Tauber, Silicon Processing For The VLSI Era, Vol. I, Second Edition, page 19, under 1.3.51 Oxygen and Carbon Measurements in Silicon Using Infrared Absorbance Spectroscopy*).

Yang teaches pertaining to claim 13, wherein the implanted oxygen ions have a peak concentration in a lower half of the silicon layer (col. 7, lines 18-26, ***Note***: the Examiner takes the position that the implanted oxygen ions would have a concentration that varies from an upper and lower surface of the silicon substrate and a concentration in a lower half of the silicon substrate, since the nature of the implantation will concentrate the ions in one part (upper or lower half) of the substrate vs. the other depending on the energy of the implant. Additionally, since silicon conventionally includes an oxygen concentration at room temperature of $2.5 \times 10^{15}/cm^3$, any additional oxygen ion implantation, within a specific region may combine with the implanted oxygen to further vary the concentration of the upper and lower surfaces of the substrate. See *Stanley Wolf and Richard N. Tauber, Silicon Processing For The VLSI Era, Vol.*

I, Second Edition, page 19, under 1.3.51 Oxygen and Carbon Measurements in Silicon Using Infrared Absorbance Spectroscopy).

Yang teaches pertaining to claim 17, wherein the first oxidation-resistant film comprises at least one of a nitride film and a photoresist film (col. 5, lines 59-65; col. 6, lines 12-18).

Yang teaches, pertaining to claim 18, further comprising: depositing a second oxidation-resistant film **20a/b** after the first oxidation-resistant film **18/a/b** has been removed from said parts of the silicon layer (figure 1; col. 6, lines 26-38); and etching the second oxidation-resistant film to leave sidewalls on vertical edges of the remaining parts of the first oxidation-resistant film before the oxygen ions are implanted (figure 1; col. 5, lines 59-65; col. 6, lines 39-43).

Yang teaches, pertaining to claim 19, wherein the second oxidation-resistant film is an oxide film or a nitride film (figure 1; col. 59-65).

Yang teaches, pertaining to claim 20, a method of fabricating a semiconductor device, comprising: providing a supporting substrate **11** having an insulating film **12** disposed thereon, and having a silicon layer **14** disposed on the insulating film (figure 1; col. 5, lines 13-17); oxidizing a surface of the silicon layer to form a pad oxide film **16** (figure 1; col. 6, lines 5-11); passing oxygen ions **22** into an upper surface of the pad oxide film, and out of a lower surface of the pad oxide film to implant the oxygen ions into selected parts of the silicon layer that are in direct contact with the lower surface of the pad oxide film, directly under, and completely covered by the pad oxide film (figure 2; col. 7, lines 10-26); and oxidizing **24** the selected parts of the silicon layer, into which the oxygen ions have been implanted, and while the selected parts are still covered by the pad oxide film, to form isolation regions dividing the silicon layer into a

plurality of mutually isolated active regions (figures 3 and 4; col. 7, lines 38-64; col. 8, lines 52-65).

Yang teaches, pertaining to claims 21, 22 and 23, wherein all parts of the silicon layer having the oxygen ions implanted therein, including the selected parts, are completely covered by the pad oxide film, and wherein during said oxidizing, the selected parts are completely covered by the pad oxide film (figure 2; col. 7, lines 10-26).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2, 3, 9 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yang et al., US Patent 6,686,255 in view of Prabhakar US Patent 5,869,359.

Yang discloses the semiconductor method substantially as claimed. See preceding rejection of claims 1, 4-6, 8, 11-13 and 17-23 under 35 U.S.C. 102(e).

However, Yang fails to show, pertaining to claims 2 and 9, wherein the silicon layer has a thickness of at most seventy nanometers. In addition, Yang fails to show, pertaining to claims 3 and 10, wherein the semiconductor device is a fully depleted silicon-on-insulator device.

Prabhakar teaches in figures 1-10, and corresponding text, a semiconductor device, including field oxide regions formed within a silicon layer. In addition, Prabhakar teaches,

pertaining to claims 3 and 10, the method wherein the semiconductor device is a fully depleted silicon-on-insulator device.

It would have been obvious to one of ordinary skill in the art to have incorporated, wherein the semiconductor device is a fully depleted silicon-on-insulator device, in the method of Yang, pertaining to claims 3 and 10, according to the teachings of Prabhakar, with the motivation that, as stated in col. 1, lines 15-27; col. 4, lines 27-57, the fully depleted SOI device taught by Prabhakar, includes the use of field oxide regions formed within the selected parts of the silicon layer, where conventional technology teaches that these regions are used for the purpose of device isolation. In addition, one of ordinary skill in the art would be drawn to use of a thin SOI layer, taught in both Yang and Prabhakar, with the motivation that, the SOI substrate produces lower parasitic capacitances for greater channel current, which in turns allows for faster switching speed. Finally, both Yang and Prabhakar teaches, the formation of the thin SOI layer to have a thickness within a range of 100 to about 2000 angstroms (10 nm to 200 nm), as a result, having a silicon layer with a thickness of at most seventy nanometers would result in routine experimentation since both the silicon layers are within the same order.

Response to Arguments

Applicant's arguments with respect to claims 1-6, 8-13 and 17-20 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stanetta D. Isaac whose telephone number is 571-272-1671. The examiner can normally be reached on Monday-Friday 9:30am -6:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Lebentritt can be reached on 571-272-1873. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Stanetta Isaac
Patent Examiner
February 13, 2006

LYNNE A. GURLEY
PRIMARY PATENT EXAMINER
TC 2800, AU 2812